

108c (metal, silicide, or other conductive material) may have a low workfunction (for example, <4.0 eV). The potential barrier height of blocking stack **120** is approximately equal to the workfunction difference between p+ a-Si:H layer **112** and conductive layer **108c**. In other embodiments, a crystalline layer material such as p+ c-Si:H **712** may be used instead of bottom i a-Si:H layer **110a** (for example, as in FIG. 7A), or p+ a-Ge:H (or some other material with a different band gap) may be added on top of (or inserted into) p+ a-Si:H layer **112** (for example, as in FIG. 8A).

Shown in FIG. 9E is Schottky HJFET **900e**. Schottky HJFET **900e** includes heterojunction gate contact **110a** and **112** and a Schottky blocking "stack" for blocking stack **120** (in this case, the "stack" is the **112/108c** Schottky junction). Top conductive layer **108c** (metal, silicide, or other conductive material) may have a low workfunction (for example, <4.0 eV, or <3.5 eV) to form a Schottky junction with p+ a-Si:H layer **112**. The potential barrier height of blocking "stack" **120** is approximately equal to the workfunction difference between p+ a-Si:H layer **112** and conductive layer **108c**. In other embodiments, a crystalline layer material such as p+ c-Si:H **712** may be used instead of bottom i a-Si:H layer **110a** (for example, as is shown in FIG. 7A), or p+ a-Ge:H (or some other material with a different band gap) may be added on top of (or inserted into) p+ a-Si:H layer **112** (for example, as is shown in FIG. 8A).

Some embodiments of the present invention recognize that: (i) in some applications of interest, such as substrate preparation by layer transfer onto glass or plastic, only one type of substrate (n or p) is available; (ii) a JFET and a MOSFET can create complementary circuits, such as an inverter, on such a substrate; (iii) with a normally-ON JFET, however, full swing of the output voltage from approximately ground (GND) to approximately supply (V_{DD}) is not possible; (iv) with the JFET structure disclosed herein, normally-OFF devices are possible; and (v) as a result of (iv), full swing is feasible.

FIG. 10A illustrates such a device in the form of inverter structure **1000**. Structure **1000** includes MOSFET **1010** and JFET **1020**, both formed on top of buried oxide (BOX) **1001**. Unlike the previous example embodiments formed on n-type substrates, structure **1000** is formed on p-type SOI c-Si substrates **1002a** and **1002b**. In addition to SOI **1002a**, MOSFET **1010** includes: n⁺ source and drain layer regions **1003a** and **1003b**; high relative permittivity (high-k) gate dielectric region **1004**; and electrode layer regions **1005**. In addition to SOI **1002b**, JFET **1020** includes: n⁺ gate layer region **1003c**; intrinsic layer **1006** and p⁺ gate layer region **1007** that together make up add-on layer **120** in this embodiment; and electrode contact layer regions **1005**. JFET **1020** is a normally-OFF device, with a $V_p < 0$ V. This structure is made practical by the inclusion of blocking stack **120** in gate stack **105** of the JFET.

Graph **1050** of FIG. 10B shows the output current characteristics as a function of gate voltage for MOSFET **1010** (line **1052**) and JFET **1020** (line **1054**). As can be seen from the Figure, a V_p of less than 0 V for JFET **1020** together with a threshold voltage (V_{TN}) greater than 0 V for MOSFET **1010** permits full-swing operation.

FIG. 11A provides another illustration of a complementary circuit device in the form of inverter **1100**. Inverter **1100** includes MOSFET **1110** and HJFET **100a** (see FIG. 1A), both formed on top of BOX **102**. Inverter **1100** is an n-type device, with both MOSFET **1110** and HJFET **100a** fabricated on top of n-type c-Si substrate layer regions **104**. The components of HJFET **100a** have been previously described. The components of p-channel MOSFET **1110**

include: 25 nm thick p⁺ hydrogenated microcrystalline Si (pc-Si:H) source and drain layer regions **1112**; 25 nm thick aluminum oxide (Al₂O₃) gate dielectric **1114**; and electrode contacts **1116**. Both the **1112** and **1114** layer regions are deposited at temperatures below 200° C. For purposes of demonstrating the application of HJFET devices to complementary circuits, MOSFET **1110** is connected externally to HJFET **100a** as shown in the Figure. Note that this p-channel MOSFETs embodiment is only intended to demonstrate the feasibility of complementary function, so neither its structure (for example, the Al₂O₃ gate dielectric) nor fabrication process as described is necessarily optimal. FIG. 11A illustrates an inverter structure formed by connecting an n-channel HJFET and a p-channel MOSFET fabricated on the same n-type c-Si substrate. Schematic **1150** of FIG. 11B shows this same circuit component combining p-MOSFET **1110** and n-HJFET **100a**, but with the structure abstracted away.

Shown in graph **1180** of FIG. 11C are the output characteristics of the HJFET/MOSFET inverter of FIG. 11A. Complementary function is observed for supply voltages as low as 1 V. The inverter gain increases from ~20 to ~40 by increasing the supply voltage from 1 V to 2.5 V. Inverter performance would likely improve by improving the p-channel MOSFET employed. While FIGS. 10A through 11C illustrated complementary circuit inverters, other circuits, such as static random access memory (SRAM) cells, pass transistors, latches, logic gates, and so on are similarly possible, as will be readily apparent to one of ordinary skill in the art in light of the present disclosure.

In all of the embodiments described herein, a back-gate electrode may be optionally included by either disposing the buried insulator (such as BOX **102**) on a conductive substrate (carrier substrate), or on a semiconductor substrate in contact with a conductive electrode. As known in the art, applying a bias voltage to the back-gate of a MOSFET modulates the Fermi level inside the channel material (such as SOI **104**), modulating the threshold voltage of the MOSFET accordingly. Similarly, applying a back-gate voltage to a JFET modulates the Fermi level in the channel material and modulates the pinch-off voltage accordingly. In some embodiments, the disclosed JFET/MOSFET inverters or other complementary circuit devices disposed on the same substrate may share a common back gate.

Devices **1200a** and **1200b** are examples of back gate embodiments of the present invention. These are presented in FIGS. 12A and 12B, respectively. Devices **1200a** and **1200b** are similar to HJFET device **100a** of FIG. 1A except for the addition of a back gate, formed by BOX **102** directly on conductive substrate **1208** (such as metal) in FIG. 12A, and by BOX **102** on semiconductor carrier substrate **1204** on conductive electrode **1208** in FIG. 12B.

FIG. 12C presents graph **1250**, showing the transfer characteristics of HJFET **1200b** (that is, having a carrier substrate). VBG is back-gate voltage and VD is drain voltage. Finally, FIG. 12D shows inverter **1280**, like inverter **1100** of FIG. 11A but with back-gate electrode formed by carrier substrate **1204** on conductive electrode **1208** (as discussed above, the carrier substrate may be omitted in some embodiments).

In some embodiments of the present invention, a thin blocking structure is incorporated in the gate stack of heterojunction field-effect transistor (HJFET) devices to substantially suppress the gate current when the gate heterojunction is forward-biased. As a result, normally-OFF HJFET devices with MOSFET-like characteristics can be obtained. The HJFET devices are comprised of gate, source and drain regions that may be formed, for example, by